

# Low Power and High Accuracy Spike Sorting Microprocessor with On-line Interpolation and Re-alignment in 90nm CMOS Process

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**Abstract**—Accurate spike sorting is an important issue for neuroscientific and neuroprosthetic applications. The sorting of spikes depends on the features extracted from the neural waveforms, and a better sorting performance usually comes with a higher sampling rate (SR). However for the long duration experiments on free-moving subjects, the miniaturized and wireless neural recording ICs are the current trend, and the compromise on sorting accuracy is usually made by a lower SR for the lower power consumption. In this paper, we implement an on-chip spike sorting processor with integrated interpolation hardware in order to improve the performance in terms of power versus accuracy. According to the fabrication results in 90nm process, if the interpolation is appropriately performed during the spike sorting, the system operated at the SR of 12.5 k samples per second (sps) can outperform the one not having interpolation at 25 ksp on both accuracy and power.

## I. INTRODUCTION

Spike sorting is an important tool to study neural activities and brain functions in neuroscience research [1]–[3]. It is also a key component in cortically-controlled neuroprosthetics to benefit spinal cord injured patients [4]. Robust sorting performance is an important issue for these applications [5]. The results of the neural decoding are less significant without an accurate spike sorting. On the other hand, making miniaturized and wireless microsystems for the experiments on free-moving subjects is one of the current research trends [6]–[13]. On the resource-constrained systems, the power minimization is required and may result in the compromise on sorting performance.

One of the design issues for the power and accuracy tradeoff is the sampling rate (SR). Since the classification of spikes depends on the features extracted from the spike waveforms, a better sorting performance usually comes with a higher SR. However the high SR leads to a larger power consumption for the recording, processing, and wireless telemetry, which may not be feasible for the applications. A SR of 100 k sample per second (sps) is recommended in [14] for an excellent spike sorting performance. However the current microsystems are usually designed with the SRs of 20 ksp or lower [7], [8], [10]–[12].

In this paper, in order to improve the power-accuracy tradeoff, we integrate the interpolation hardware into the

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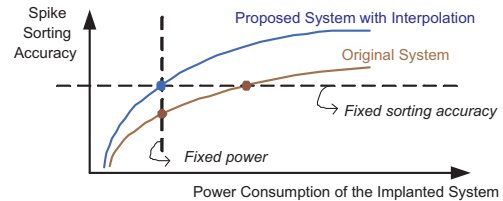


Fig. 1. The interpolation can be utilized to improve the power-accuracy tradeoff of the spike sorting microsystem. With a fixed SR and power consumption of the neural recorder, our spike sorting system achieves higher sorting accuracy through the interpolation. With an anticipated sorting accuracy, the implanted system consumes less power with a lower SR after the interpolation.

spike sorting microsystem. Since most spike energy is under 6.25 kHz [14], after the waveform reconstruction through the interpolation, the sorting performance with 100 ksp signal resolution could be achieved even if the neural recorder has a low SR for low power consumption. The improvement of the systems can be interpreted in two different aspects as shown in Fig. 1. With a fixed SR and the corresponding power consumption, the interpolation improves the sorting accuracy of the systems. On the other side, after the interpolation, an anticipated sorting accuracy may be achieved with a lower SR as well as a lower power consumption.

After the proof-of-concept algorithm simulation [15] and the circuit design of interpolation hardware [16], we will focus more on the system integration and implementation results in this paper. The remainder of the paper is organized as follows. The spike sorting microsystem is introduced in Section II. In Section III, we will show how to efficiently integrate the interpolation to the neural recording and spike sorting microsystem to improve the accuracy-power tradeoff. Section IV shows the implementation results, and Section V concludes this work.

## II. SPIKE SORTING MICROSYSTEMS

### A. Neural Recording and Spike Sorting

Most neurons in the brain communicate by firing action potentials, or spikes. These electrical voltage signals can be recorded extracellularly with very thin electrodes implanted into brains. Very often an implanted electrode records the signals from multiple surrounded neurons, and the recorded waveform is the superimposed potentials generated by these neurons. Spike sorting is a kind of reverse process to differ-

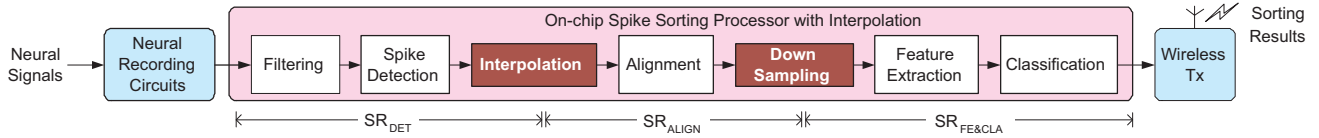


Fig. 4. The proposed on-chip spike sorting system with interpolation hardware. The system is divided into three stages with different SRs.  $SR_{DET}$ ,  $SR_{ALIGN}$ , and  $SR_{FE&CLA}$  represents the data SRs used by the stages of spike detection, alignment, and feature extraction along with classification.

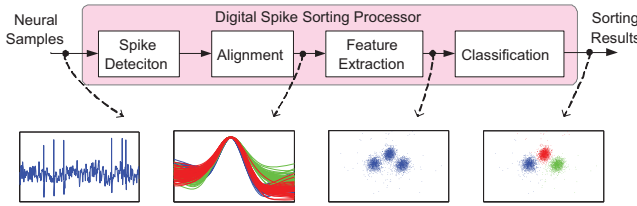


Fig. 2. The hardware modules of the spike sorting microsystem.

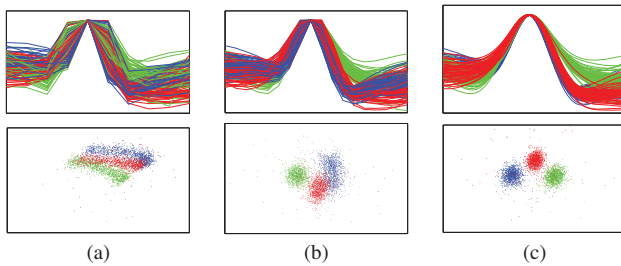


Fig. 3. The improvement of neuron cluster separation after the interpolation. The original neural signals are sampled at 12.5 kps and aligned according to the peak as shown in (a). For (b) and (c), the spike waveforms are re-aligned after the up-sampling to 25 kps and 100 kps with the cubic spline interpolation. The synthesized neural data of “C\_Difficult1\_noise01” from [17], [18] are adopted. Different colors is used for different neurons according to the golden standards (not the classified results). The features used in the lower figures are the first two principal components after the haar wavelet transformation of the spikes.

entiate which spike corresponds to which of these close-by neurons from the superimposed waveform.

Figure 2 shows the hardware modules of the spike sorting. After the frontend neural recording circuitry amplifies and digitizes the microvolt neural potentials, the neural samples are input to the digital processor for spike sorting. The spikes are usually detected according to their localized instantaneous energy. Then the waveform characteristics, or the features, of the spikes are extracted after the waveform alignment. Spikes with similar features should be corresponding to one specific neuron. Therefore, the spikes are classified according to the assembled clusters on the finite-dimension feature space.

### B. Sampling Skew and Power-accuracy Tradeoff

The sorting of the spikes are usually based on the differentiation of the spike shapes and the extracted features. As a result, any waveform variation during the recording may result in significant degradation on sorting performance. Sampling skew is one of the main causes for the waveform variations. During the neural recording, the sampling of the

neural signals is discrete. The hardware can hardly sample the spikes at exactly the same points of the waveform characteristics. The time difference, or the so-called sampling skew, results in the the variation of the spike waveforms and affect the sorting performance. The most obvious variation are happened in the neural polarization and depolarization regions (i.e. peak and valley) which are the waveform characteristics generally used for spike sorting.

A common solution for the sampling skew is to increase the sampling frequency. The SR of 100 kps may be required by the system asking for extremely high-end sorting performance [14]. However, for portable or implantable neural recorders supporting a large channel number, low power consumption is essential. The system with high SR usually leads to a large power consumption and is not feasible for the applications. Therefore, the SR of 20 kps or lower is generally adopted in the current hardware designs with the compromise on the accuracy of spike sorting.

## III. PROPOSED SPIKE SORTING MICROSYSTEMS WITH CUBIC SPLINE INTERPOLATION

### A. Interpolation

The spikes have the most energy under 6.25 kHz. According to the Nyquist-Shannon sampling theory, it should be feasible to reconstruct the 100 kps spike waveforms through the interpolation if the SR is higher than 12.5 kps. An uncompromised spike sorting performance may thus be achieved even with a SR as low as 12.5 kps. Figure 3 shows the improvement of the neuron separation by means of the interpolation. The neural signals are originally sampled at 12.5 kps and aligned according to the peak as shown in Fig. 3 (a). Then the spike waveforms are interpolated to 25 kps and 100 kps in Fig 3 (b) and (c) respectively. After the interpolation, the peaks of the neural spikes are reconstructed, and the waveform can be re-aligned with less error caused by the sampling skew. This improves the separation of neuron clusters on the feature space and leads to a better sorting performance. For the algorithm analysis of the using of cubic spline interpolation, please refer to [15].

### B. On-chip Spike Sorting Microsystem with Interpolation

In the proposed system, the interpolation hardware is integrated to improve the power-accuracy tradeoff. Although the interpolation hardware requires the additional power, it allows the system to use the recording frontend circuits with a lower SR in some respects. Since the power consumed by the recording frontend chips [7] is about an order larger than the state-of-the-art spike sorting designs [10], [11], the

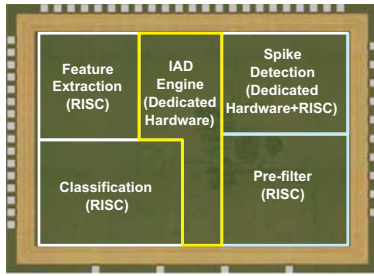


Fig. 5. Chip micrograph of the proposed spike sorting microprocessor with interpolation hardware. The IAD engine performs the interpolation, alignment, and downsampling as shown in Fig. 4.

TABLE I  
SYNTHESIZED RESULTS IN 90 NM CMOS PROCESS

Process	90 nm 1P9M Low-leakage CMOS
Supply Voltage	1.0 Volt
Operation Frequency	20 MHz in Maximum
Chip Area	8.89 (3.50x2.54) mm <sup>2</sup>
Core Area	5.92 (2.96x2.00) mm <sup>2</sup>
Power Consumption	87.02 $\mu$ W (0.68 $\mu$ W/channel)*

\*The power consumption is measured under the parameters of 45  $\frac{\text{samples}}{\text{spike}}$  and 20  $\frac{\text{spikes}}{\text{channel} \times \text{sec}}$  for 128 channels.  $\{SR_{DET}, SR_{ALIGN}, SR_{FE\&CLA}\}$  are set to  $\{12.5, 50, 25\}$  ksp. The algorithms running on the microprocessor are NEO spike detection, DWT-PCA feature extraction, and k-means classifier.

power tradeoff after the interpolation would finally result in a smaller total power.

Further, even after the interpolation, some power consumption in spike sorting processor can also be saved if the high signal resolution is only utilized at the critical step of the spike sorting. Figure 4 shows the architecture of the proposed spike sorting processor. The processor is divided into three stages with different SRs for the specific purposes. In the first stage, spike detection usually uses the energy detector and does not need detailed waveform information. Therefore the low SR ( $SR_{DET}$ ) can be used in this stage. In the second stage, the interpolation is first performed and the detected spikes can be aligned with a higher SR ( $SR_{ALIGN}$ ) in order to reduce the sampling skew and improve the ability of neuron separation. In the third stage, the feature extraction and classification are operated after the down-sampling. Since the sampling skew is minimized during the high-resolution alignment, there should be relatively small waveform variations after the down-sampling. A lower SR ( $SR_{FE\&CLA}$ ) can thus be used to minimize the power consumption.

#### IV. IMPLEMENTATION RESULTS

The proposed spike sorting microprocessor shown in Fig. 4 is implemented and fabricated in 90 nm CMOS low-leakage process. We use reduced instruction set computer (RISC) to construct most of the processing modules in order to preserve the programmability for various spike sorting algorithms. The cubic spline interpolation [16] along with the alignment and downsampling are implemented in a dedicated parallel hardware called IAD engine. Configurations to turn on and off the interpolation engine are designed to compare the

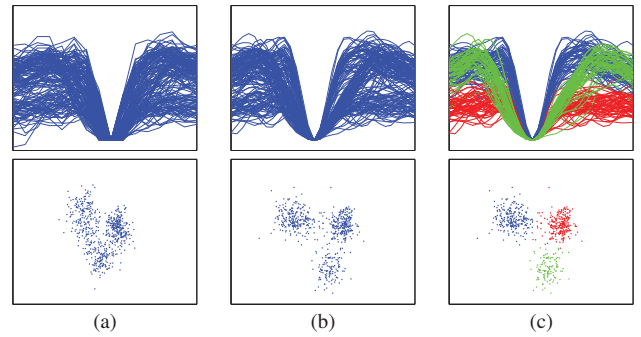


Fig. 6. The processing results of the chip. The inputs are pre-recorded neural signals from the rat hippocampus [19], [20]. The fourth channel in the data set of d1122206 is used. Different hardware configurations for the IAD engine are programmed to demonstrate the accuracy with and without the interpolation. (a)  $SR_{DET} = SR_{ALIGN} = SR_{FE\&CLA} = 12.5$  ksp. (b)  $\{SR_{DET}, SR_{ALIGN}, SR_{FE\&CLA}\} = \{12.5, 50, 25\}$  ksp. (c) The spike sorting results of (b) after K-means classification algorithm.

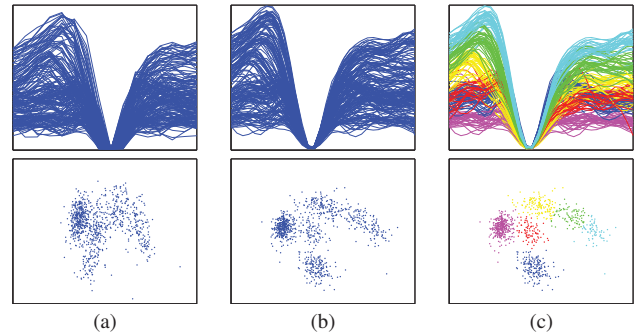


Fig. 7. The processing results of the chip. The inputs are pre-recorded neural signals from the rat hippocampus [19], [20]. The fourth channel in the data set of d14521.001 is used. Different hardware configurations for the IAD engine are programmed to demonstrate the accuracy with and without the interpolation. (a)  $SR_{DET} = SR_{ALIGN} = SR_{FE\&CLA} = 12.5$  ksp. (b)  $\{SR_{DET}, SR_{ALIGN}, SR_{FE\&CLA}\} = \{12.5, 100, 50\}$  ksp. (c) The spike sorting results of (b) after K-means classification algorithm.

spike sorting performance and power consumption with and without the interpolation. The RISCs and IAD engine are cascaded as a processing pipeline and operated simultaneously. Figure 5 shows the die micrograph of the chip. Table I summarizes the chip implementation results.

Figure 6 and Fig. 7 show some testing results of the chip with the pre-recorded neural signals from rat hippocampus [19], [20]. The data are downsampled to 12.5 ksp for the chip testing. The NEO spike detection, DWT-PCA feature extraction, and K-means classification algorithms are coded in assembling language, compiled to the machine code, and programmed onto the chip. Note that the algorithm parameters such as threshold in spike detection, projection vectors of PCA, and so on are trained off-line with the PC. Different configurations for the IAD engine are tested and compared to demonstrate the accuracy improvement of the spike sorting after the interpolation. In Fig. 6 and 7 (a), the IAD engine is turned off. Because of the related low SR and large sampling skew, the boundary of different clusters of the detected spikes can hardly be seen on the feature space. In Fig. 6 and Fig. 7 (b), the IAD engine is turned on.

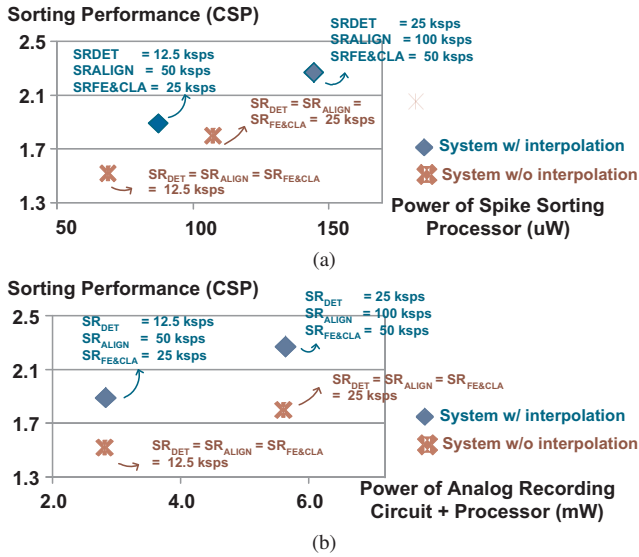


Fig. 8. The comparison for power and sorting accuracy (CSP, cluster separation parameter) between different hardware configurations. The CSP values is from our previous works of [15]. The power of analog recording frontend is estimated from [8].

Because the sampling skew is reduced, the boundary of the clusters are more distinguishable. Figure 6 and 7 (c) shows the corresponding classification results.

Figure 8 shows the improvement of the sorting accuracy versus power consumption. In this comparison, the sorting accuracy is referred from our previous algorithm analysis work in [15]. The power of spike sorting processor is measured from the chip. The power of analog recording circuit is estimated from [8], in which 4.4 mW is required for the amplifiers and ADCs in 128 channels and 20ksp/s. We linearly normalized the number with the sampling frequency in this comparison. Four configurations of spike sorting processor are tested as follows: (A)  $\{SR_{DET}, SR_{ALIGN}, SR_{FE\&CLA}\} = \{12.5, 50, 25\}$  ksp/s; (B)  $\{SR_{DET}, SR_{ALIGN}, SR_{FE\&CLA}\} = \{25, 100, 50\}$  ksp/s; (C)  $SR_{DET} = SR_{ALIGN} = SR_{FE\&CLA} = 12.5$  ksp/s; (D)  $SR_{DET} = SR_{ALIGN} = SR_{FE\&CLA} = 25$ . The configuration (A) and (B) represents the system with interpolation. The configuration (C) and (D) represents the system without interpolation. Clearly, in Fig. 8 (a), the spike sorting processor with interpolation (A and B) has a better accuracy-power curve compared to the processor without IAD engine (C and D). In Fig. 8 (b), the power consumption of analog recording circuits is further included. After the interpolation, A can achieve similar or even better sorting performance than D and consumes less power consumption.

## V. CONCLUSION

In this paper, the spike sorting processor with interpolation is proposed to improve the performance in terms of sorting accuracy versus power consumption. The idea is implemented and fabricated in 90nm low-leakage CMOS process. The results show that the system in 12.5 ksp/s SR outperforms the system in 25 ksp/s on both accuracy and

power if the interpolation is appropriately utilized in the spike sorting.

## REFERENCES

- [1] M. Abeles and M. H. Goldstein, "Multispikes train analysis," *Proceedings of the IEEE*, vol. 65, no. 5, pp. 762–773, 1977.
- [2] J. Carmenta, M. Lebedev, R. E. Crist, J. E. O'Doherty, D. M. Santucci, D. Dimitrov, P. Patil, C. S. Henriquez, and M. A. Nicolelis, "Learning to control a brain-machine interface for reaching and grasping by primates," *PLoS Biology*, vol. 1, no. 2, pp. 193–208, 2003.
- [3] M. Velliste and et al., "Cortical control of a prosthetic arm for self-feeding," *Nature*, vol. 453, pp. 1098–1101, 2008.
- [4] Z. Zumsteg, C. Kemere, S. O'Driscoll, G. Santhanam, R. Ahmed, K. Shenoy, and T. Meng, "Power feasibility of implantable digital spike sorting circuits for neural prosthetic systems," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 13, no. 3, pp. 272–279, 2005.
- [5] M.D. Linderman, G. Santhanam, C.T. Kemere, V. Gilja, S. O'Driscoll, B.M. Yu, A. Afshar, S.I. Ryu, K.V. Shenoy, and T.H. Meng, "Signal processing challenges for neural prostheses," *IEEE Signal Processing Magazine*, vol. 25, no. 1, pp. 18–28, 2008.
- [6] R. H. Olsson and K. D. Wise, "A three-dimensional neural recording microsystem with implantable data compression circuitry," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2796–2804, 2005.
- [7] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, 2007.
- [8] M. Chae, W. Liu, Z. Yang, T.-C. Chen, J. Kim, M. Sivaprakasam, and M. Yuce, "A 128-channel 6mW wireless neural recording ic with on-the-fly spike sorting and uwb transmitter," in *Proceeding of IEEE International Solid-State Circuits Conference*, Feb 2008, pp. 146–603.
- [9] T. C. Chen, K. Chen, Z. Yang, K. Cockerham, and W. Liu, "A biomedical multiprocessor soc for closed-loop neuroprosthetic applications," in *Proceeding of IEEE International Solid-State Circuits Conference*, Feb. 2009, vol. 25, pp. 434–435.
- [10] V. Karkare, S. Gibson, and D. Markovic, "A 130-gw, 64-channel spike-sorting dsp chip," in *Proceeding of IEEE Asian Solid-State Circuits Conference*, 2009, pp. 289–292.
- [11] T.-C. Chen, W. Liu, and L.-G. Chen, "128-channel spike sorting processor with parallel-folding structure in 90nm process," in *Proceeding of IEEE International Symposium on Circuits and Systems*, 2009, pp. 1253–1256.
- [12] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni, "An activity-dependent brain microstimulation SoC with integrated 23nV/rtHz neural recording front-end and 750nW spike discrimination processor," in *IEEE Symposium on VLSI Circuits*, 2010, pp. 223–224.
- [13] S. Gibson, J. W. Judy, and D. Markovic, "Technology-aware algorithm design for neural spike detection, feature extraction, and dimensionality reduction," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, to appear.
- [14] T. J. Blanche and N. V. Swindale, "Nyquist interpolation improves neuron yield in multiunit recordings," *Journal of Neuroscience Methods*, vol. 155, no. 1, pp. 81–91, 2006.
- [15] Y.-Y. Chen, T.-C. Chen, and L.-G. Chen, "Accuracy and power tradeoff in spike sorting microsystems with cubic spline interpolation," in *Proceeding of IEEE International Symposium on Circuits and Systems*, 2010, pp. 1508–1511.
- [16] T.-C. Chen, Y.-Y. Chen, T.-C. Ma, and L.-G. Chen, "Design and implementation of cubic spline interpolation for spike sorting microsystems," in *Proceedings of IEEE International Conference on Acoustics, Speech, and Signal Processing*, 2011, pp. 1641–1644.
- [17] R. Q. Quiroga, "Simulated multi-unit extracellular recordings," <http://www2.le.ac.uk/departments/engineering/extranet/research-groups/neuroengineering-lab/software>.
- [18] R. Q. Quiroga, Z. Nadasdy, and Y. Ben-Shaul, "Unsupervised spike detection and sorting with wavelets and superparamagnetic clustering," *Neural computation*, vol. 16, pp. 1661–1687, 2004.
- [19] G. Buzsaki, "Physiological data from the rat hippocampus," <http://ccrns.org/data-sets/hc/hc-1/>.
- [20] K.D. Harris, D.A. Henze, J. Csicsvari, H. Hirase, and G. Buzsaki, "Accuracy of tetrode spike separation as determined by simultaneous intracellular and extracellular measurements," *Journal of Neurophysiology*, vol. 84, no. 1, pp. 401V414, 2000.